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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

00201242.5

Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

I.L.C. HATTEN-HECKMAN

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Blatt 2 der B scheinigung
Sheet 2 of the certificate
Page 2 de l'attestation

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Application no.: 00201242.5
Demande n°:

Anmeldetag:
Date of filing: 05/04/00
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Anmelder:
Applicant(s):
Demandeur(s):
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Bezeichnung der Erfindung:
Title of the invention:
Titre de l'invention:
A method and apparatus for testing digital circuitry through a loop-back from a buffered data output to a buffered control input or vice versa whilst executing a Built-In-Self-Test methodology

In Anspruch genommene Prioriät(en) / Priority(ies) claimed / Priorité(s) revendiquée(s)

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Internationale Patentklassifikation:
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Am Anmeldetag benannte Vertragstaaten:
Contracting states designated at date of filing: AT/BE/CH/CY/DE/DK/ES/FI/FR/GB/GR/IE/IT/LI/LU/MC/NL/PT/SE/TR
Etats contractants désignés lors du depôt:

Bemerkungen:
Remarks:
Remarques:

A method and apparatus for testing digital circuitry through a loop-back from a buffered data output to a buffered control input or vice versa whilst executing a **Built-In-Self-Test** methodology.

BACKGROUND OF THE INVENTION

The invention relates to a method for testing digital circuitry as recited in the preamble of Claim 1. In general, digital full swing high speed data transmission between two integrated circuit chips necessitates the use of a wide-frequency spectrum. Therefore, actual data transmission is very frequency sensitive. To reduce frequency sensitivity, it is better to send an analog low swing bit stream instead of digital data. Now, for sending analog bit streams, an analog low swing interface (**LSI**) is necessary; note that this abbreviation has a different meaning from everyday usage in electronic technology. To ensure correct functionality of this interface it is these low swing interface signals should be rendered digitally testable. However, a standard manufacturing test machine cannot handle the analog input and analog output signals. Therefore, a specific test interface facility should be provided, for executing the actual digital manufacturing tests.

SUMMARY TO THE INVENTION

In consequence, amongst other things, it is an object of the present invention to provide a test facility that in the context of a loop-back configuration will be able to straightforwardly communicate test and/or result patterns to/from the intended destinations and/or sources while minimizing various items thereof with respect to cost, complexity, bandwidth, frequency sensitivity and other parameters that would burden a test manager.

Now therefore, according to one of its aspects the invention is characterized according to the characterizing part of Claim 1.

The invention also relates to an apparatus being arranged for implementing a method as recited in Claim 1. Further advantageous aspects of the invention are recited in dependent Claims.

BRIEF DESCRIPTION OF THE DRAWING

These and further aspects and advantages of the invention will be discussed more in detail hereinafter with reference to the disclosure of preferred embodiments, and in particular with reference to the appended Figures that show:

Figure 1, an archetypical test configuration;

Figure 2, a prior art loop-back test system;

Figure 3, the LSI device in normal mode;

Figure 4, the test interface of Figure 3's circuitry in actual test mode.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 1 diagrammatically illustrates an archetypical test configuration. Herein, **TESTER** block 30 generates and provides test patterns through interconnection facility 32 to the **D**evice **U**nder **T**est 34. After execution of the test, the results of the test through interconnection facility 32 return to the tester block for evaluation, which may result in *reject*, *repair*, or *pass* in whole or in part. Tester block 30 may be either a separate device or may be wholly or partially integrated with the device under test. For brevity, external usage of the test results has not been shown in the Figure.

Figure 2 diagrammatically illustrates a prior art loop-back test system as disclosed more fully in US Patent 5,787,114, and in particular, Figure 3 thereof. Here, under non-test circumstances, parallel digital output patterns (9) are presented to a transmitter (5), serialized (11), buffered (15), clocked (14), and outputted (6) on a P/N wire pair. Also, serial digital input patterns received on a P/N wire pair (7) are buffered (16), deserialized (12), clock-extracted (17) and/or reference-clocked (REFCLK), aligned (18), and presented as parallel input patterns (4). Under test conditions, a switch (19) is closed for effecting loop-back, whereas switch (25) is opened for effecting insulation from the outer world. A **B**uilt-**I**n-**S**elf-**T**est unit (20) may, through generating a wrap-back control (22) and in cooperation with a switch (23) effect a wrapback (10) from the data alignment unit (18) to the serializer (11), thereby effectively limiting the test procedures to only the I/O interface facilities. Furthermore, an interconnection (26) with Alignment unit 18 has been shown. For additional detail, reference is had to the full prior art specification.

Figure 3 shows the **L**ow **S**wing **I**nterface circuitry to be tested still in normal mode, with a conceptual interface 50 that communicates analog signals between the first comprehensive chip actually shown and a further chip with an appropriate interface not shown. The interface to the outer world numbers a Transmit/Receive (RxTx) pair, one for data signals (52) and one for control signals (54). For effecting bidirectional transmission, each time an input lead has been joined to an output lead. No further chip has been shown for brevity.

In contradistinction to the above, the core functionality at right in the Circuit comprises by way of example a **D**igital **P**rocessing **M**aster **U**nit (62) in which the data handling functionality proper is effected, a **S**erial **I**nput/**O**utput unit 64, and a **D**igital **S**ignal **P**rocessor 66 that is serially and bidirectionally interconnected to **SIU** 64. Clocking of the latter is effected through gate M3 (58) that gets control signals as well as data signals. As shown for brevity, SIU only operates as a data source with respect to the outer world. Furthermore, gate M1 (56) presents data to DFMU (62), and synchronizing signals to gate M3 (58). Gate M2 (57) presents data to the outer world, as received from DFMU 62 and SIU 64. In similar manner, control signals are communicated between LSI 54 and gates M3 (58) and M4 (60).

In this setup, the analog transmitter circuits Tx will convert the digital full swing signal into an analog low swing signal. In its turn, the analog receiver will transform the low swing analog signal back into a full swing digital signal. In fact, a digital production test machine is not capable to evaluate the analog signals, so that effectively, the instant test interface solves a pressing problem.

In the setup, communication between the two chips necessitates at least two of the interface arrangements. Of these, the first one (54) will send the control signals on two paired full-differential lines. The second interface (52) effects data transmission on two further likewise paired full-differential lines. To save power and to suppress unwanted self-coupling and instability, the Rx of the transmitting LSI is in power-off mode, for data signals just as for control signals. Otherwise, the Tx is switched off while receiving. Therefore, one control signal, not shown for brevity, is needed for every Low Swing Interface circuit. Now, with this prior art test interface there are three different operating modes:

Transmitting, with Tx on and Rx off.
Receiving, with Tx off and Rx on.
Testing, with both Tx and Rx on.

The providing of these three modes necessitates extra design effort for the power control circuit of the LSI under test, and moreover, for each LSI a second control wire is necessary for effecting these three modes, inasmuch as a single wire is insufficient.

In this respect, Figure 4 illustrates the test interface of the present invention operating in actual test mode. Generally, elements 52, 54, 56, 57, 58, 60, 62, 64, 66 correspond to those of Figure 3. The above two disadvantages are now avoided by this low power for a low swing interface. Such has been effected by the cross-coupling of both

interfaces. In consequence, there are now only two conditions for every LSI circuit, as follows:

Transmitting, with Tx on and Rx off.

Receiving, with Tx off and Rx on.

Having only these two modes renders it much easier to save power. As shown, Switches 53 and 53 provide loop-back between data transmitter and control receiver, and between control transmitter and data receiver, respectively. Each of these two is controlled by a single bit as has been indicated on control line 67. Such is also the case for the control LSI and data LSI themselves. The control is provided by block 66 in the lower right corner of the Figure. Furthermore, the appropriate number of control bits has been indicated with respect to the various gates 56, 57, 58, 60. Gate M2 (57) needs only one control bit to select between standard data out and test data out. Gate M1 (56) needs two control bits to select between standard data in and test data in, on the one hand, and between various different sources, on the other hand, four possibilities in total in this embodiment as indicated. Likewise, Gate M4 (60) needs two control bits to select between standard data out and test data out, on the one hand, and between various different destinations, on the other hand, three possibilities in total in this embodiment as indicated. Likewise, Gate M3 (58) needs three control bits to select between standard data in and control in, on the one hand, and between various different sources, on the other hand, four? possibilities in total in this embodiment as indicated.

CLAIMS:

1. A method for testing digital circuitry through effecting a paired loop-back from a first buffered output to a first buffered input whilst within the circuitry executing at least part of the test through using a **Built-In-Self-Test** methodology,

characterized by effecting said loop-back from the first buffered data output to a buffered control input.

2. A method for testing digital circuitry through effecting a paired data loop-back from a first buffered output to a first buffered input whilst within the circuitry executing at least part of the test through using a **Built-In-Self-Test** methodology,

characterized by effecting said loop-back from a buffered control output to the first buffered data input.

3. A method as claimed in Claim 1, characterized by effecting said loop-back from a buffered control output to the first buffered data input.

4. A method as claimed in Claims 1, 2 or 3, whilst in connection with said buffering executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry.

5. A method as claimed in Claims 1, 2 or 3, whilst controlling both said loop-back as well as said buffering through a one-bit control signal.

6. A method as claimed in Claim 5, whilst controlling signal routing between said buffering on the one hand, and test circuitry as well as core circuitry of said digital circuitry, on the other hand, through a plural bit control signal.

7. An apparatus arranged for implementing a method as claimed in Claim 1, for testing digital circuitry provided with a paired loop-back from a first buffered output to a first buffered input associated with an in-circuit **Built-In-Self-Test** facility,

characterized by having said loop-back effected from the first buffered data output to a buffered control input.

8. An apparatus arranged for implementing a method as claimed in Claim 1, for testing digital circuitry provided with a paired data loop-back from a first buffered output to a first buffered input associated with an in-circuit Built-In-Self-Test facility,

characterized by having said loop-back effected from a buffered control output to the first buffered data input.

9. An apparatus as claimed in Claim 7, characterized by having said loop-back effected from a buffered control output to the first buffered data input.

10. An apparatus as claimed in Claims 7, 8 or 9, provided with conversion means for in connection with said buffering executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry.

11. An apparatus as claimed in Claims 7, 8 or 9, wherein both said loop-back as well as said buffering have a one-bit control signal input.

ABSTRACT:

Digital circuitry is tested through effecting a paired data loop-back from a first buffered output to a first buffered input whilst within the circuitry executing at least part of the test through using a **B**uilt-**I**n-**S**elf-**T**est methodology. In particular, the loop-back is effected from the first buffered data output to a buffered control input, from a buffered control output to the first buffered data input, or both. Advantageously, the buffering is associated to executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of the digital circuitry.

Figure 4

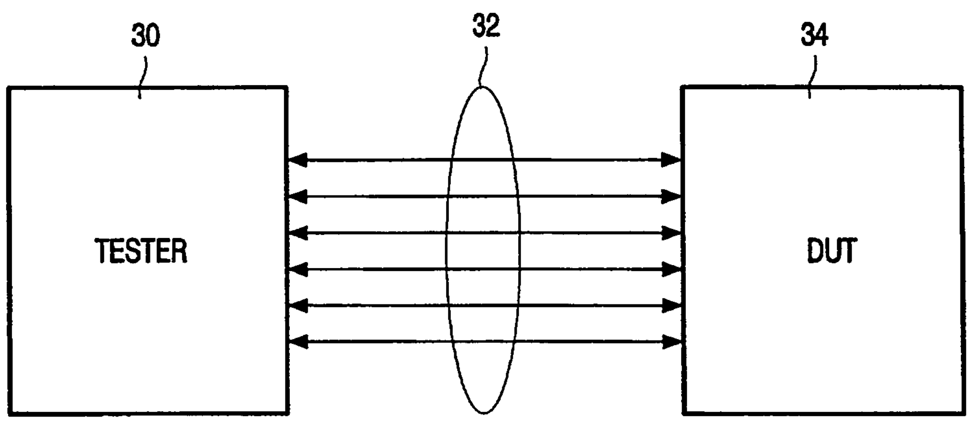
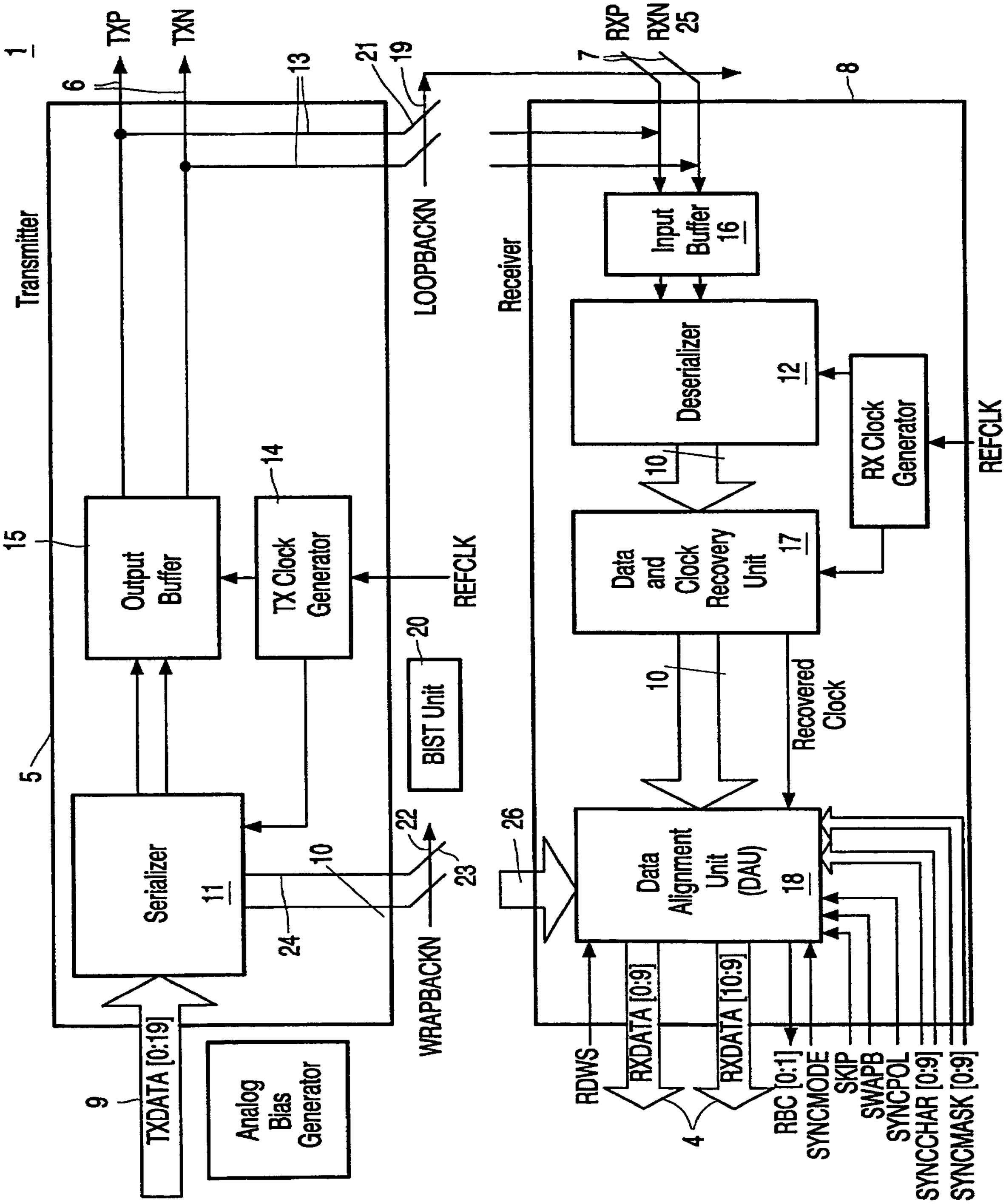


FIG. 1


TXP
TXN
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Output Buffer
TX Clock Generator
REFCLK
Serializer 11
BIST Unit
LOOPBACKN
WRAPBACKN
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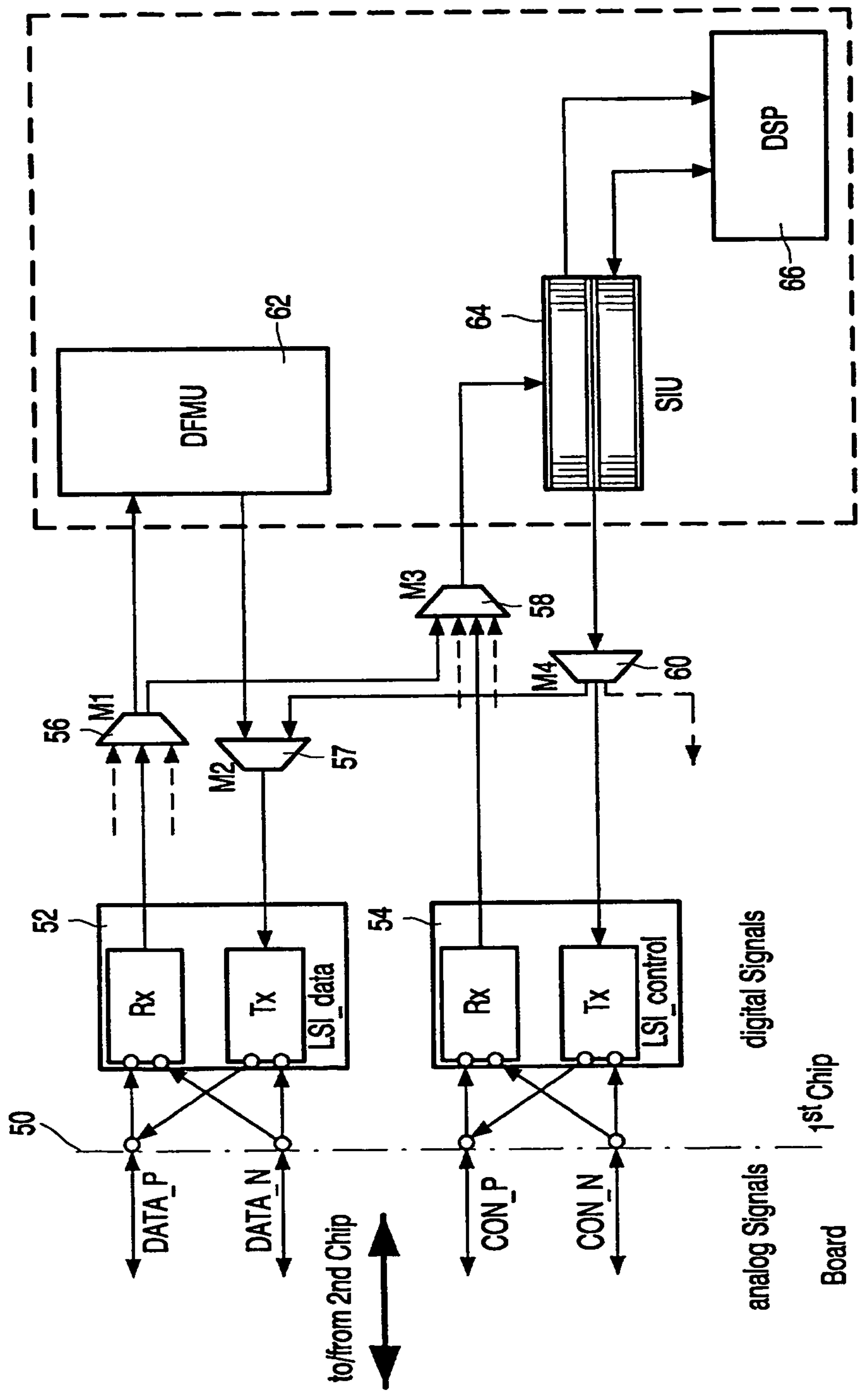
Analog Bias Generator
RXP
RXN
Receiver
Input Buffer 16
Deserializer 12
RX Clock Generator
REFCLK
Data and Clock Recovery Unit 17
Recovered Clock
Data Alignment Unit (DAU) 18
RDWS
RXDATA [0:9]
RXDATA [10:9]
RBC [0:1]
SYNCMODE
SKIP
SWAPB
SYNCPOL
SYNCCHAR [0:9]
SYNCMASK [0:9]

FIG. 2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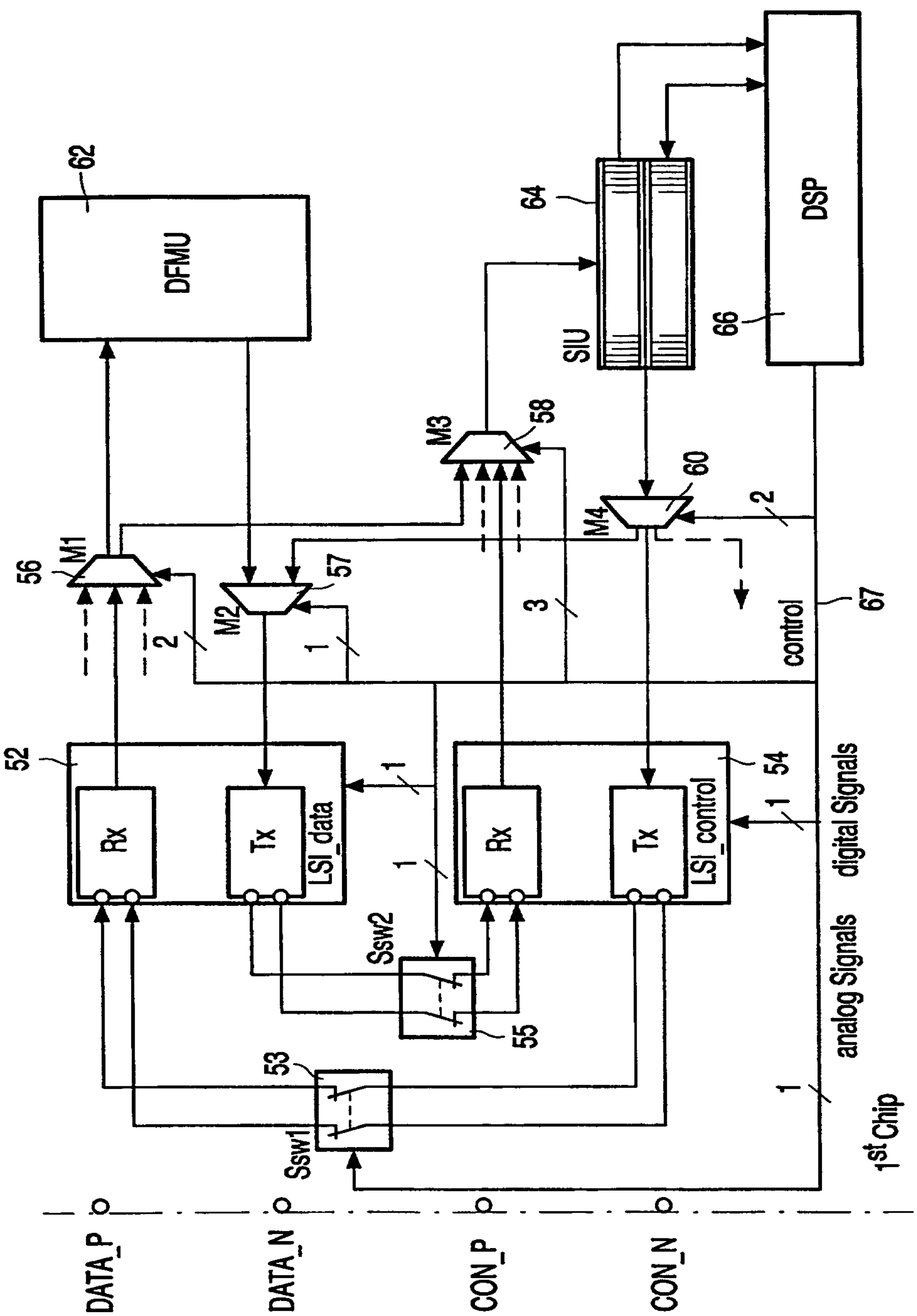
64
SIU
DFMU
62
M3
58
M4
60
56
M1
M2
57
52
Rx
Tx
LSI_data
54
Rx
Tx
LSI_control
digital Signals
50
1st Chip
DATA_P
DATA_N
CON_P
CON_N
analog Signals
Board
to/from 2nd Chip

FIG. 3



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Ssw2
55
control
67
digital Signals
analog Signals
1st Chip
DATA_P
DATA_N
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CON_N
1
2
3

FIG. 4